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THERMAL CYCLE TESTING OF 7-SEGMENT LIGHT EMITTING DIODES (LED) --ETC(U)
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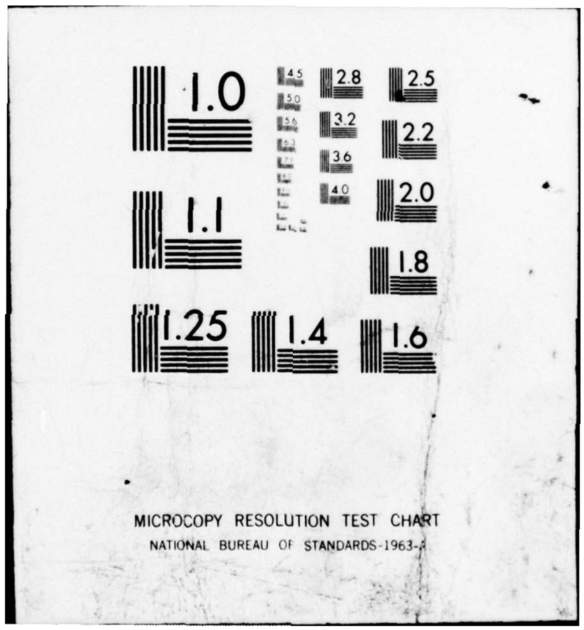
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RESEARCH AND DEVELOPMENT TECHNICAL REPORT
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THERMAL CYCLE TESTING OF 7-SEGMENT LIGHT EMITTING DIODES (LED) DISPLAYS
(Test Evaluation)

M. Robert Miller
Electronics Technology & Devices Laboratory

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Extended thermal cycle tests were performed on four types of LED numeric displays following observation of device failure during testing of equipment containing these displays. Two types which were epoxy encapsulated had failure rates of 1 percent and 0.17 percent per thermal cycle. No failures were observed in hermetically sealed devices or the devices that were potted in a resilient material.

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THERMAL CYCLE TESTING OF 7-SEGMENT LIGHT EMITTING DIODES (LED) DISPLAYS

(Test Evaluation)

INTRODUCTION

Military electronic equipment can be expected to experience hundreds of thermal cycles during its operational lifetime when it is exposed to temperature extremes such as the low temperatures encountered at high altitudes and arctic environments, and the high temperatures encountered in tropical environments and in enclosed spaces under sunloading. Thermal cycle tests consisting of just a few cycles between temperature extremes are usually adequate to uncover most types of failure mechanisms due to thermal mismatch; however in situations where the effects of thermal cycling are cumulative, more extensive evaluation must be performed. The structure of plastic encapsulated LED numeric displays represents such a case and the work described in this report was performed to determine the cumulative nature of the effect, and to compare the responses of other structures to this stress. This problem surfaced in the AN/APN-209 (Absolute Altimeter) Engineering Development program when several LED failures were observed during the reliability demonstration. The preliminary analysis determined that the failure mechanism was tearing of the lead wires between the segments caused by differential thermal expansion of the epoxy encapsulant/lead wire structure. The AN/APN-209 contractor attempted a solution to the problem by purchasing unencapsulated LED numerics and potting them in a resilient material (Sylgard MC 7384). Samples of these were included in this test along with hermetically packaged devices and two types of epoxy encapsulated devices.

TEST PROCEDURES

The test was performed according to test condition A of Method 107D of MIL-STD-202E. Two temperature chambers were used, one at -55 degrees Celsius (°C), and the other at +85°C. The devices were shuttled back and forth between the chambers by hand, spending 15 minutes at each temperature extreme with a typical transfer time of 2 minutes. About 14 cycles could be completed per day. Once each day, power was applied to the devices and the number of segment failures was visually noted. The test was terminated after 158 cycles. The total test period was 16 days. The general layout of the devices during the test is shown in Figure 1 which also served as a record of the test results. The numbers recorded next to some of the segments represent the number of cycles that had been completed when the failure of that segment was observed. No distinct geographical pattern emerges among these failures other than the complete lack of failures in the soft potted (Type III) and hermetic (Type IV) units.

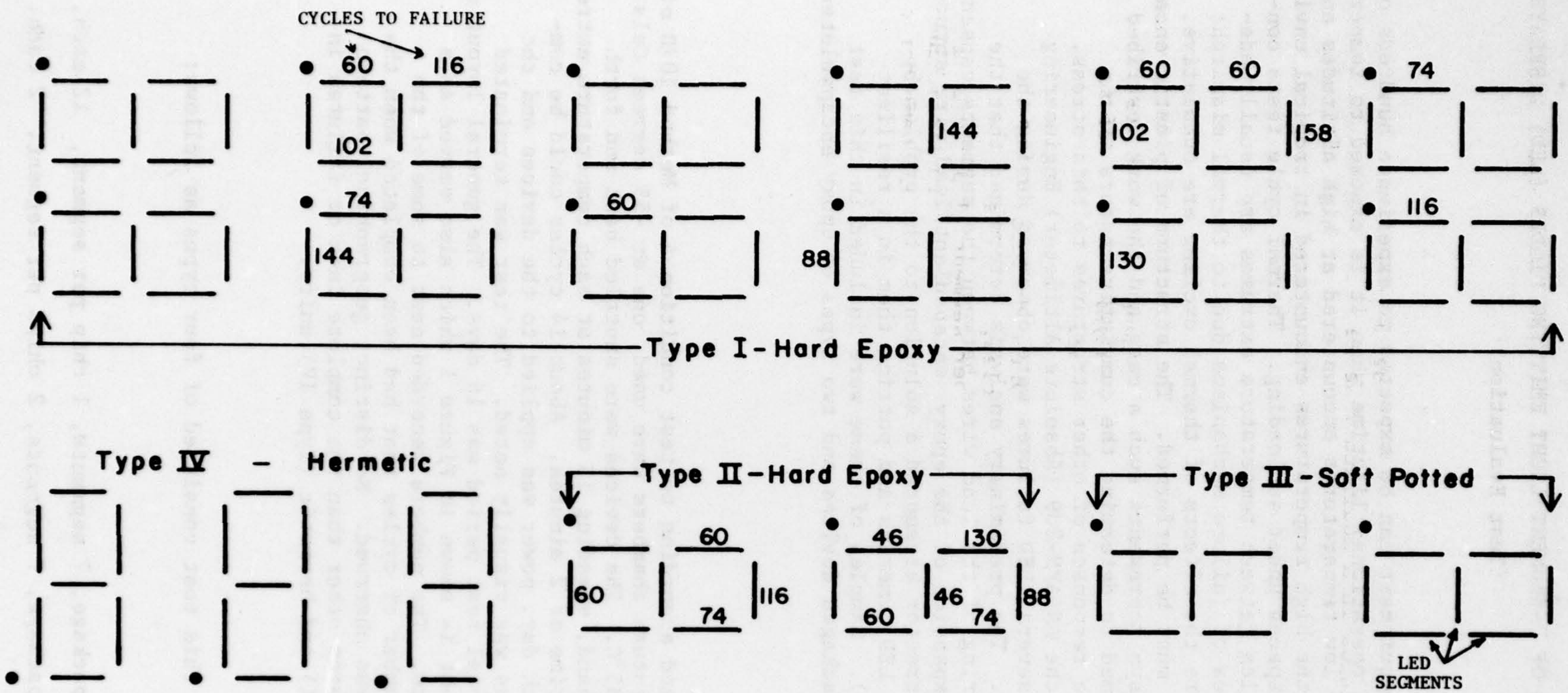
TEST DEVICES

The devices used in this test consisted of four types as follows:

TYPE

I. Hard epoxy package, 7 segments, 1 chip per segment, 12 each.

II. Hard epoxy package, 7 segments, 2 chips per segment, 2 each.



Step
1— -55°C 15 min
2— 25°C 5 min (max)
3— 85°C 15 min
4— 25°C 5min(max)

Figure 1. LED Numeric Display Thermal Shock Test. Method 107D Test Condition A MIL-STD-202E.

TYPE (Contd.)

III. Obtained unencapsulated and potted with Sylgard. Otherwise same as Type II, 2 each.

IV. Hermetically sealed package including decoding and drivers with 27 LED chips in a modified 7 segment format, 3 each.

RESULTS

Because the individual segments of a seven segment LED numeric are effectively independent devices, each segment was considered separately, resulting in a meaningful statistical sample size. In the case of the hermetic devices which include decoding and drive circuitry inside the package so that individual segments are not independently accessible electrically, any failures would have required analysis in terms of the whole circuit. However this situation did not occur.

The first failures occurred in the hard epoxied devices with 2 chips per segment (Type II) after 46 cycles. After 60 cycles, failures began to appear in the hard epoxied devices with 1 chip per segment (Type I). Failures continued to accumulate in these two types throughout the remainder of the test period as shown by the curves of Figure 2. Throughout this same period, no failures were observed in either the hermetic devices (Type IV) or Sylgard potted devices (Type III).

ANALYSIS

An exponential failure distribution was assumed of the form:

$$f = 1 - e^{-\lambda n}$$

where; $f \times 100$ is the cumulative failure percentage,
λ is the failure rate per thermal cycle, and
n is the number of thermal cycles.

The data of Figure 2 can be matched to such a curve by the least squares method with a high degree of correlation. Rearranging the above equation as:

$$-\ln(1-f) = \lambda n$$

and letting; $x = n$
$y = -\ln(1 - f)$,
then $y = \lambda x$.

We can solve for λ by using a least squares linear regression of the form:

$$\lambda = \frac{N \Sigma x_i y_i - \Sigma x_i \Sigma y_i}{N \Sigma x_i^2 - (\Sigma x_i)^2}$$

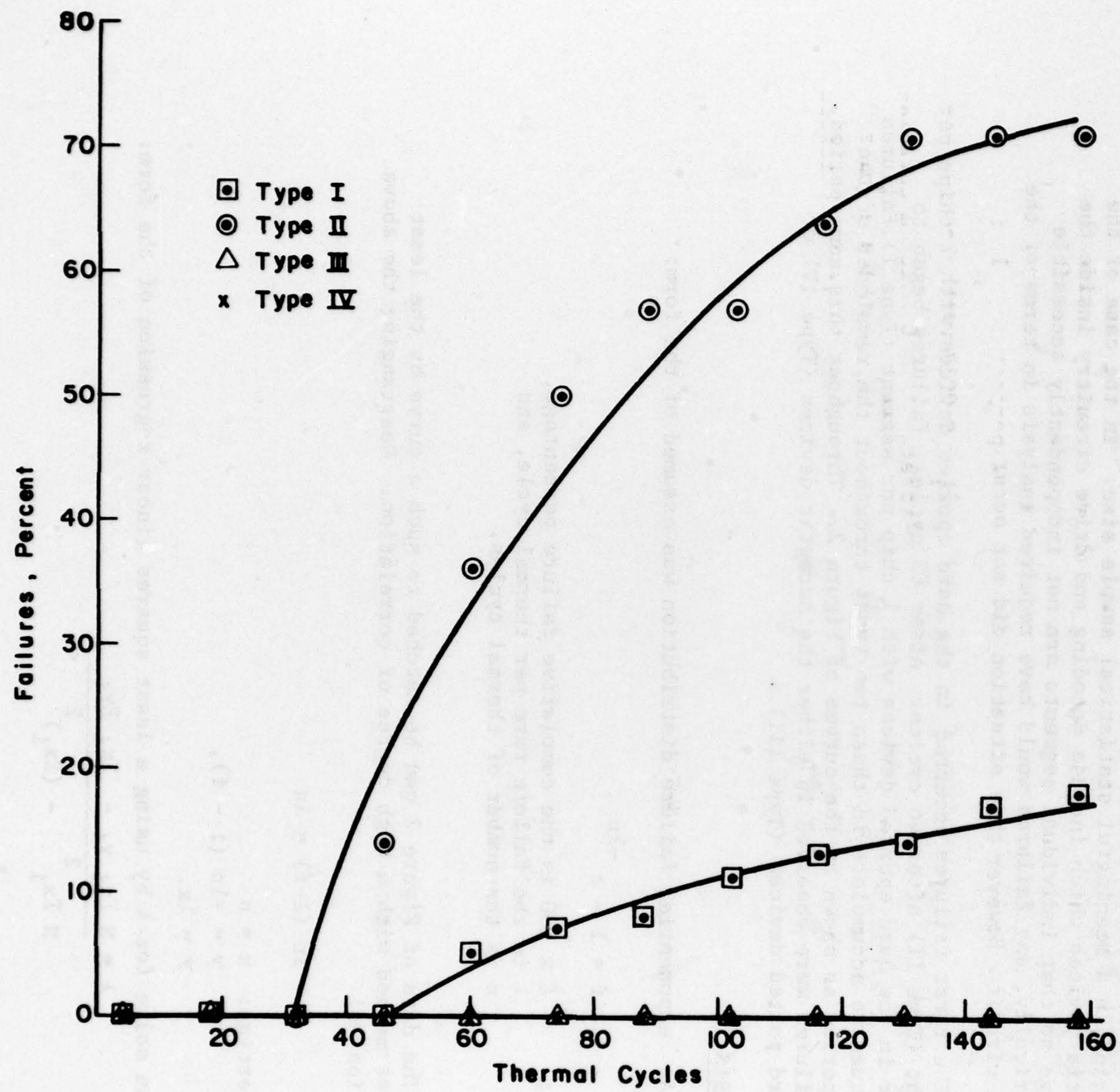


Figure 2. Graph of Cumulative Segment Failures.

where x_i and y_i are the coordinates of the N data points.

The correlation of the data points to the resulting equation is given by:

$$\gamma = \frac{N\Sigma x_i y_i - \Sigma x_i \Sigma y_i}{\sqrt{(N\Sigma x_i^2 - (\Sigma x_i)^2)(N\Sigma y_i^2 - (\Sigma y_i)^2)}}$$

where, $0 \leq \gamma \leq 1$ with a value of 1 representing perfect correlation.

For the Type I device, the data yields $\lambda_I = 0.0017$ with a correlation coefficient $\gamma_I = 0.99$. For the Type II device, $\lambda_{II} = 0.01$ with a correlation coefficient $\gamma_{II} = 0.97$. These correlation coefficients are quite good considering the limited sample sizes that were used. It is therefore not unreasonable to conclude that these hard epoxy potted devices demonstrated constant failure rates of 0.17 percent per cycle and 1.0 percent per cycle respectively, and this can be compared to the hermetic and soft potted units in which no failures were induced by this test procedure.

The differences in the failure rates between Types I and II probably derive from structural differences between the units such as:

Type I	Type II
1 chip/segment	2 chips/segment
single wire bond/chip	redundant bonding
structured encapsulation (see Figure 3)	homogeneous encapsulant

Some features of the test results should be noted in conjunction with these structural differences. First, the use of redundancy, as in the redundant bonding of the Type II devices does not, by itself, guarantee high reliability. Also, the structured encapsulation of the Type I devices shown in Figure 3, which was designed primarily on the basis of optical considerations, is essentially the same as the homogeneously encapsulated devices with respect to the region around the lead wire where the breakage occurs.

The effects of particular structural features were not studied but, between them, these two types are fairly representative of almost all of the hard epoxy encapsulated LED numeric displays on the market today. The real significance lies in the comparison of these two types of units with the soft potted and hermetically sealed devices.

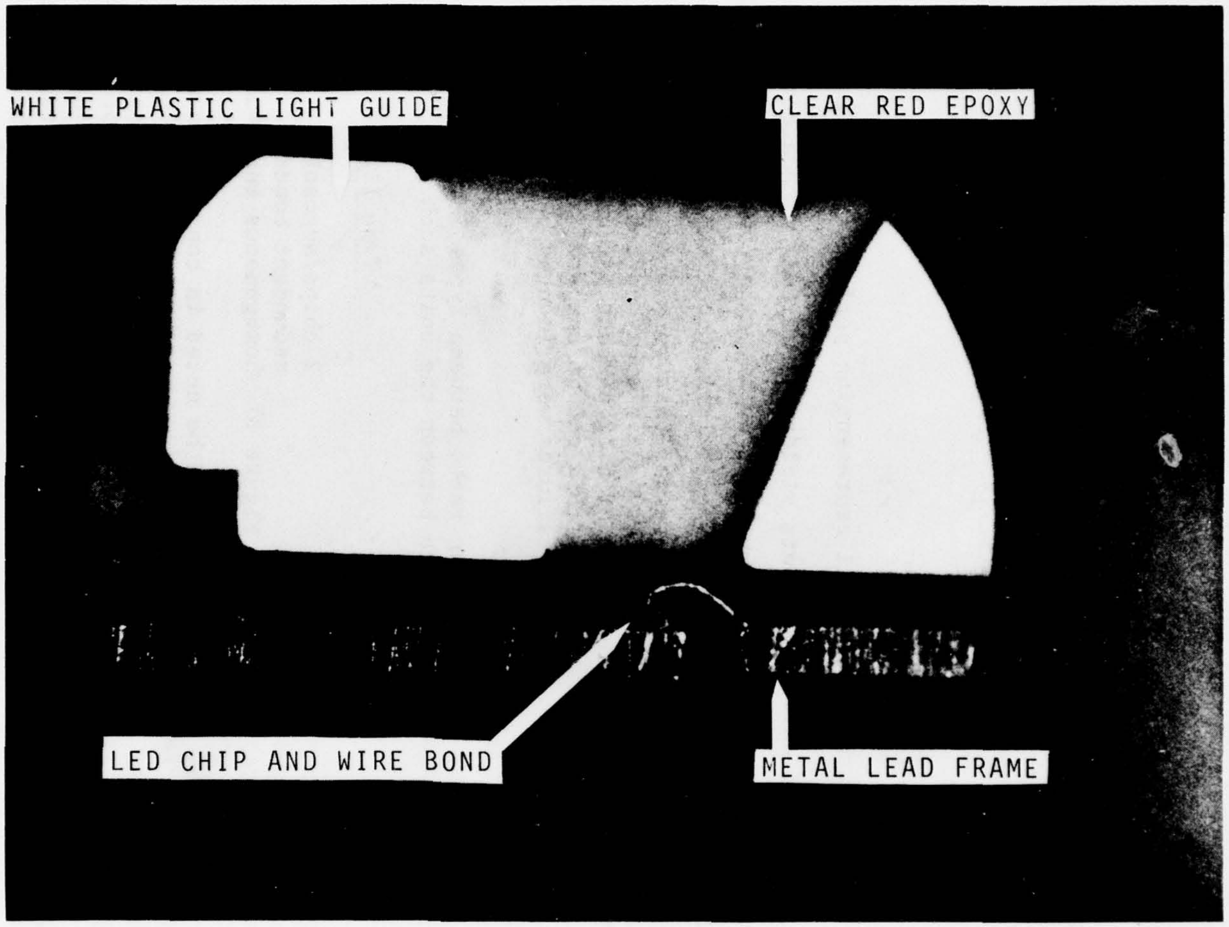


FIGURE 3. PHOTOGRAPH OF A SECTIONED TYPE I DEVICE

CONCLUSIONS

Although the sample size used in this test was too small to allow quantitative predictions of reliability, the consistency of the results leads to rather definite conclusions about the nature of the failure mechanisms. The complete absence of failures in the hermetic and soft-potted units clearly identifies epoxy potting as the source of the problem; and the constant failure rates measured for the epoxy potted units eliminate early failures or end of life types of failures from consideration. Instead, it appears that the effects of thermal cycling are cumulative at a constant rate that depends upon the device structure.

Since epoxy potting is the packaging method used for most of the LED numeric display devices on the market at present, it is incumbent on systems developers to insure that the temperature environment be considered during system design and steps be taken to avoid thermal cycling failures.

Also to be considered is the tendency for manufacturers and even most military specifications to call for relatively few (less than 10) thermal cycles as part of the reliability testing. Obviously, this is not sufficient to uncover cumulative thermal problems.

The data given here is based on a set of test conditions that is appropriate for many military applications. For other applications, in which less severe temperature extremes are expected, further evaluation will be needed to determine the relationship between failure rate and temperature.

Additional experimentation could also be considered to determine the effects of various potting compositions, but for immediate application where thermal cycling is an important consideration, these results indicate two approaches that appear acceptable. Hermetic devices are available off-the-shelf at a somewhat higher cost than the potted devices. Sylgard potting is not normally done by the device manufacturers but could be considered if the appropriate capabilities are available.

In the case of the AN/APN-209, the solution that was adopted for production of this equipment involving about 10,000 digits, was to purchase unpotted units from the device manufacturer, and to have the units potted in Sylgard by the contractor.

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